AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A programmable logic controller (PLC), comprising:

a first processing unit, which executes low-speed pulse outputs, low-speed counting, and first group commands; and

a second processing unit, which takes an interrupt signal generated by the first processing unit to execute a corresponding high-speed pulse output, high-speed counting, and a second group command;

wherein the second processing unit includes a basic command executing module for executing the second group command;

wherein the basic command executing module further includes:

an internal memory unit, which stores the second group commands;

a logic operation unit, which is coupled to the internal memory unit for executing the second group command; and

a flag accumulating unit, which is coupled to the logic operation unit and, after the second group command is executed, changes a flag value in the flag accumulating unit.

2-4. (Cancelled)

5. (Currently Amended) ~~The PLC of claim 4,~~ A programmable logic controller (PLC), comprising:

a first processing unit, which executes low-speed pulse outputs, low-speed counting, and first group commands; and

a second processing unit, which takes an interrupt signal generated by the first processing unit to execute a corresponding high-speed pulse output, high-speed counting, and a second group command;

wherein the second processing unit includes a pulse output module for output a plurality of high-speed pulse signals;

wherein the pulse output module comprises:

a pulse output start module, which outputs a start signal;

a pulse width modulation (PWM) module, which is coupled to the pulse output start module, starts when the start signal is a PWM start signal, and outputs a PWM pulse signal;

a pulse output module, which is coupled to the pulse output start module, starts when the starts signal is the pulse output module start signal, and output a pulse signal; and

a speed-reduced pulse output module, which is coupled to the pulse output start module, starts when the start signal is a speed-reduced pulse output module start signal, and outputs a speed-reduced output pulse signal.

6. (Cancelled)

7. (Currently Amended) ~~The PLC of claim 6,~~ A programmable logic controller (PLC), comprising:

a first processing unit, which executes low-speed pulse outputs, low-speed counting, and first group commands; and

a second processing unit, which takes an interrupt signal generated by the first processing unit to execute a corresponding high-speed pulse output, high-speed counting, and a second group command;

wherein the second processing unit includes an interrupt module for outputting interrupt signals.

wherein the interrupt module ~~contains~~includes:

an interrupt enable flag, which records an interrupt enable flag value;

a positive/negative edge setting flag, which records one of an up-rising edge interrupt and a lowering edge interrupt;

a start unit, which is coupled to the interrupt enable flag and is actuated by the interrupt enable flag output and an interrupt source to output a start signal;

a positive/negative edge detector, which is coupled to the start unit for receiving the start signal and outputs a positive/negative edge detection signal according to the positive/negative edge setting flag;

an interrupt vector start buffer, which is coupled to the positive/negative edge detector for storing an interrupt vector state;

an interrupt state determiner, which uses the interrupt vector state and the output of an interrupt vector capture buffer to determine whether an up-rising edge interrupt or a lowering edge interrupt is detected; and

an interrupt state device, which is coupled to the interrupt state determiner for outputting an interrupt signal according to the determination result of the interrupt state determiner.

8. (Cancelled)

9. (Currently Amended) ~~The PLC of claim 8,~~ A programmable logic controller (PLC), comprising:

a first processing unit, which executes low-speed pulse outputs, low-speed counting, and first group commands; and

a second processing unit, which takes an interrupt signal generated by the first processing unit to execute a corresponding high-speed pulse output, high-speed counting, and a second group command;

wherein the second processing unit includes a counting module for executing a plurality of high-speed counting modes;

wherein the counting module includes:

a counter comparison value recording unit, which stores a counter comparison value;

a counter current value recording unit, which stores a counter current value;

a counting comparison unit, which is coupled to the counter comparison value recording unit for comparing the counter comparison value and the counter current value to determine whether the former value (U value) or the latter value (D value) reaches a predetermined value;

a ~~de-multiplexier~~de-multiplexer, which is coupled to the counting comparison unit and, when the counting comparison unit outputs a logic signal representing the predetermine value, outputs a counting mode signal to the basic command executing module;

a U/D detecting unit, which is coupled to the counter current value recording unit for receiving the counter current value to determine whether the current counting number is the U value or the D value and outputs a detection result; and

a ~~de-multiplexier~~de-multiplexer, which is coupled to the U/D detecting unit for using the detection result along with the counting mode to output the signal to the basic command executing module.

10. (Currently Amended) ~~The PLC of claim 1,~~ A programmable logic controller (PLC), comprising:

a first processing unit, which executes low-speed pulse outputs, low-speed counting, and first group commands; and

a second processing unit, which takes an interrupt signal generated by the first processing unit to execute a corresponding high-speed pulse output, high-speed counting, and a second group command;

wherein the second processing unit includes a counting module for executing a plurality of high-speed counting modes;

wherein the second processing unit includes a comparison counting module.

11. (Currently Amended) The PLC of claim 10, wherein the comparison counting module ~~contains~~includes:

a comparison result output address unit, which stores comparison result output addresses;

a comparison mode setting unit, which stores comparison mode settings;

a counting comparison setting value unit, which stores counting comparison setting values;

a ~~de-multiplexier~~ de-multiplexer, which receives the output signal from the counting module and outputs a counting content; and

a sixth comparator, which is coupled to the comparison result output address unit for comparing the counting content and the counting comparison value setting and outputs a comparison result to a ~~de-multiplexier~~de- multiplexer.